CLAIMS

1. An apparatus comprising:

a circuit configured to be tested; and

a plurality of test blocks within said circuit each comprising (i) a plurality of sequential elements and (ii) a plurality of logic elements, wherein (i) each of said test blocks are configured to operate (a) in a first mode comprising a shift mode and (b) a second mode comprising a capture mode, (ii) said shift mode operates with multiple scan clocks that are clocked simultaneously, and (iii) said capture mode operates with multiple scan clocks with only one of the scan clocks being toggled at a time.

2. The apparatus according to claim 1, wherein said shift mode and said capture mode comprise portions of static timing analysis.

3. The apparatus according to claim 1, wherein one of said test blocks includes a latch at an end of said plurality of sequential elements.

4. The apparatus according to claim 1, wherein said shift mode comprises simultaneously toggling all of said scan clocks.

5. The apparatus according to claim 1, wherein said capture mode comprises pulsing one of said scan clocks at a time.

6. The apparatus according to claim 1, wherein each of said sequential elements comprises a flip-flop.

7. The apparatus according to claim 1, wherein said apparatus fixes timing violations in response to said shift mode and said capture mode.

8. The apparatus according to claim 1, wherein said apparatus executes (i) a first test run in said shift mode and (ii) a second and third test run in said capture mode.

9. The apparatus according to claim 8, wherein said apparatus inserts one or more false path statements between each of said test runs.

10. A method for performing static timing analysis comprising the steps of:

(A) implementing a plurality of test blocks each comprising (i) a plurality of test elements and (ii) a plurality of logic elements; and

(B) operating in (i) a capture mode using multiple scan clocks with only one of the scan clocks being toggled at a time; and (ii) a shift mode using multiple scan clocks being toggled at a time.

11. The method according to claim 10, wherein step (B) comprises:

executing a first test run in said shift mode; and

executing a second and a third test run in said capture mode.

12. The method according to claim 11, further comprising the step of:

fixing timing violation errors in response to said test run.

13. The method according to claim 11, further comprising the step of:

inserting one or more false path statements between each of said execution steps.

14. An apparatus for performing static timing analysis comprising the steps of:

means for implementing a plurality of test blocks each comprising (i) a plurality of test elements and (ii) a plurality of logic elements; and

means for operating in a capture mode using multiple scan clocks with only one of the scan clocks being toggled at a time; and

means for operating in a shift mode using multiple scan clocks being toggled at a time.